

**ASYMMETRIC BAND-GAP ENGINEERED
NONVOLATILE MEMORY DEVICE**

Abstract of the Disclosure

5 Systems and methods are provided for nonvolatile memory devices that
incorporate a band-gap engineered gate stack with asymmetric tunnel barriers. One
embodiment of a memory device includes first and second source/drain regions
separated by a channel region in a substrate, a control gate, and a gate stack between
the control gate and the channel region. The gate stack includes a first insulator
10 region in contact with the channel region, a floating charge-storage region in contact
with the first insulator region, and a second insulator region in contact with the
floating charge-storage region and the control gate. The gate stack includes selected
material, in conjunction with control gate metallurgy, for providing desired
asymmetric energy barriers that are adapted to primarily restrict carrier flow during
15 programming to a selected carrier between the control gate and the floating charge-
storage region, and to retain a programmed charge in the floating charge-storage
region. Other aspects are provided herein.

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